

WHAT IS CLAIMED IS:

1 1. A phase-locked loop circuit for providing an output signal having a
2 frequency depending on the frequency of a reference signal, the circuit including
3 means for deriving a feedback signal from the output signal, means for providing
4 a control signal indicative of a phase difference between the reference signal and
5 the feedback signal, means for controlling the frequency of the output signal
6 according to the control signal, and means for causing the circuit to enter a lock
7 condition when the reference signal and the feedback signal have the same
8 frequency and a pre-defined phase difference means for causing the circuit to
9 enter the lock condition includes means for conditioning the control signal to
10 have an instantaneous value substantially zero in the lock condition by means of
11 a conditioning signal consisting of a series of pulses each one corresponding to
12 the pre-defined phase difference.

1 2. The circuit according to claim 1, wherein the means for providing the
2 control signal includes means for generating a phase indicator signal consisting
3 of a series of pulses each one indicative of a phase difference between the
4 reference signal and the feedback signal, and wherein the means for conditioning
5 includes means for adding the conditioning signal to the phase indicator signal,
6 the pulses of the phase indicator signal being opposite to the pulses of the
7 conditioning signal in the lock condition.

1 3. The circuit according to claim 2, wherein the means for generating
2 the phase indicator signal includes means for setting a first indicator signal in
3 response to a switching edge of the reference signal, means for setting a second
4 indicator signal in response to the switching edge of the feedback signal, means
5 for resetting the first indicator signal and the second indicator signal in response
6 to the setting of both the first and the second indicator signals, and means for
7 combining the first indicator signal and the second indicator signal into the phase
8 indicator signal, the switching edges of the reference signal and of the feedback
9 signal being synchronous with the pulses of the conditioning signal in the lock
10 condition.

1 4. The circuit according to claim 1, wherein the means for conditioning
2 includes means for generating the pulses of the conditioning signal

3 synchronously with a selected one between the reference signal and the
4 feedback signal.

1 5. The circuit according to claim 4, wherein the selected signal
2 consists of the feedback signal, the means for generating the conditioning signal
3 including means for deriving the conditioning signal from the output signal.

1 6. The circuit according to claim 5, wherein the means for deriving the
2 conditioning signal from the output signal includes means for generating the
3 switching edge and a further switching edge of each pulse of the conditioning
4 signal in response to a first switching edge and to a second switching edge,
5 respectively, of the output signal, the second switching edge of the output signal
6 corresponding to the switching edge of the feedback signal and the first switching
7 edge of the output signal preceding the second switching edge of the output
8 signal by a pre-defined number of periods of the output signal.

1 7. The circuit according to claim 6, wherein the means for generating
2 the feedback signal includes a multi-modulus divider (for deriving a pre-scaled
3 signal from the output signal, the means for deriving the conditioning signal from
4 the output signal being clocked by the pre-scaled signal.

1 8. The circuit according to claim 1, wherein the phase-locked loop
2 circuit is of a fractional type.

1 9. In a phase-locked loop circuit, a method of providing an output
2 signal having a frequency depending on the frequency of a reference signal, the
3 method including the steps of:

4 deriving a feedback signal from the output signal,

5 providing a control signal indicative of a phase difference between the
6 reference signal and the feedback signal,

7 controlling the frequency of the output signal according to the control
8 signal, and

9 causing the circuit to enter a lock condition when the reference signal and
10 the feedback signal have the same frequency and a pre-defined phase
11 difference,

12 wherein causing the circuit to enter the lock condition includes:

13 conditioning the control signal to have an instantaneous value substantially
14 zero in the lock condition by means of a conditioning signal consisting of a series
15 of pulses each one corresponding to the pre-defined phase difference.

1 10. A phase-locked loop for producing an output signal, comprising:
2 a first circuit operable to produce a first signal characterizing a phase
3 difference between a feedback signal and a reference signal; and
4 a second circuit coupled to the first circuit, the second circuit operable to
5 produce a second signal, the second circuit further operable to couple the second
6 signal to the first signal to produce a control signal having an instantaneous value
7 substantially equal to zero.

1 11. The loop of claim 10 wherein the control signal produces a locked
2 condition of the loop.

1 12. The loop of claim 10 wherein the second signal has a rising edge
2 corresponding to a rising edge of the feedback signal.

1 13. The loop of claim 10 wherein the second signal has a falling edge
2 corresponding to a rising edge of the feedback signal.

1 14. The loop of claim 10 wherein the second circuit comprises a current
2 source.

1 15. The loop of claim 14 wherein the second circuit further comprises a
2 switch operable to transition between conducting and non-conducting states, the
3 switch further operable to couple the current source to ground when in the
4 conducting state.

1 16. The loop of claim 15 wherein the second circuit further comprises a
2 third circuit operable to produce a third signal, the third signal operable to control the
3 switch transitions.

1 17. The loop of claim 16 wherein the third circuit produces the third signal
2 from the output signal.

1 18. The loop of claim 16, further comprising a fourth circuit operable to
2 produce a fourth signal from the output signal, wherein the fourth signal clocks the
3 third circuit.

1 19. A method of locking a phase-locked loop, comprising:
2 producing a first signal characterizing a phase difference between a feedback
3 signal and a reference signal;
4 producing a second signal; and
5 producing a control signal comprising the first and second signals, the control
6 signal having an instantaneous value substantially equal to zero.

1 20. An electronic system, comprising:
2 a phase-locked loop for producing an output signal, comprising:
3 a first circuit operable to produce a first signal characterizing a phase
4 difference between a feedback signal and a reference signal; and
5 a second circuit coupled to the first circuit, the second circuit operable to
6 produce a second signal, the second circuit further operable to couple the second
7 signal to the first signal to produce a control signal having an instantaneous value
8 substantially equal to zero.